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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,547	11/08/2001	Cosmin Iorga	1543-US	6760

7590 03/23/2006

Legal Department
Teradyne, Inc.
321 Harrison Avenue
Boston, MA 02118

EXAMINER	
GUTIERREZ, ANTHONY	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/010,547	IORGA, COSMIN	
	Examiner	Art Unit	
	Anthony Gutierrez	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *12-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 12-15 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

These claims are drawn to the multiplexer of claim 11, and while they further limit the multiplexer, they do not further limit the device-interface board (that includes a multiplexer) drawn to in claim 11, from which they all ultimately depend.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierzchala et al. (United States Patent 5,959,872), in view of Applicant's admitted prior art.

As to claims 1, 6, and 11, Pierzchala et al. discloses a multiplexer including a plurality of inputs, switching circuitry coupled to the input, the switching circuitry having respective outputs coupled to a common node, the switching circuitry operative to

enable a selected one of the plurality of inputs (col. 7, lines 38-55 and Fig.7), a local signal converter having a circuit branch set to a common voltage (col. 18, lines 6-11 and col. 31, lines 52-62), the branch connected to the common node to sense changes in current corresponding to an input signal received by an enabled input, and an output coupled to the local signal converter, whereby the local signal converter is operative to produce voltage changes at the output corresponding to the sensed current changes (col. 6, lines 6-23 and col. 19, lines 29-31). The multiplexer is part of a mixed (analog/digital) circuit, which is a semiconductor device, called an FPAA (col. 4, lines 47 and 48).

Pierzchala et al. does not specifically teach that this semiconductor device is used with a device-interface-board for calibration/validation of automatic test equipment, the device-interface-board including: at least one test socket adapted for receiving a device-under test.

The Applicant's admitted prior art, however, teaches these features including the adaptation to use a plurality of input pins (Specification page 1, columns 9-28), as part of automatic test equipment that plays a crucial role in the fabrication of semiconductor devices.

It therefore would have been obvious to one of ordinary skill in the art at the time of invention, to use the semiconductor device multiplexer FPAA, disclosed by Pierzchala et al., in the device-interface board configuration, as taught by Applicant's admitted prior art, in order to allow a manufacturer to functionally test the FPAA, ensuring device operability at pre-set specifications prior to entering the marketplace.

As to claims 2, 3, 7, 8, 12, and 13, Pierzchala et al. discloses that the switching circuitry comprises diodes that correspond to the inputs (Fig. 7 (G)).

As to claims 4, 9, 14, Pierzchala et al. discloses that the local signal converter comprises: a transresistance amplifier (col. 17, lines 7-11 and col. 18, lines 6-11).

As to claims 5, 10, and 15, Pierzchala et al. discloses that the transresistance amplifier includes: a base terminal fixed to a constant voltage; an emitter branch coupled to the common node; and a collector terminal tied to the output pin (col. 19, lines 16-18 and col. 19, lines 24-36).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

United States Patent Application: US 2002/0048826 A1, to Richmond, II et al., teaches a wafer level burn-in and electrical test system and method for use with a PCB.

United States Patent: US 6,535,766 B1, to Thompson et al., teaches a method of micro-electromechanical filtering for an implanted medical device.

United States Patent US 6,272,669 B1, to Anderson et al., teaches in the Background of the Invention, that an FPAA is a programmable semiconductor device.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Gutierrez whose telephone number is (571) 272-2215. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AG
Anthony Gutierrez

3/17/06

CAROL S.W. TSAI
PRIMARY EXAMINER